

**Amendments to the Claims**

1. (*Currently Amended*) A method of forming ~~electrical connection means~~ electrical connections on a substrate, comprising the following steps:

- a) depositing an intermediate layer of material  $[(14)]$  on a substrate,
- b) forming an etching mask  $[(16)]$  on the intermediate layer  $[(14)]$ , said mask having at least one window  $[(18)]$  having dimensions which are larger than the dimensions envisaged for the ~~connection means~~ electrical connections to be realized,
- c) etching the intermediate layer of material  $[(14)]$  through the window  $[(18)]$  of the mask in order to form therein at least one aperture  $[(20)]$ , having lateral side-walls, for receiving the ~~connection means~~ electrical connections,
- d) coating the lateral side-walls of the aperture with a spacer  $[(22)]$  in order to narrow the aperture,
- e) depositing at least one conductor material  $[(24)]$  so as to fill the narrowed aperture, and
- f) performing an abrasion operation in order to remove excess conductor material outside the narrowed aperture.

2. (*Currently Amended*) A method as claimed in claim 1, in which the step a) utilizes a dielectric material for forming the intermediate layer  $[(14)]$  while a metallic conductor material  $[(24)]$  is used in the step e).

3. (*Currently Amended*) A method as claimed ~~in one of the claims 1 or 2~~, in claim 1, in which the step d) comprises the deposition of a layer  $[(22)]$  of an insulating coating material, followed by the anisotropic etching of this layer so as to preserve a part thereof on the side-walls of the aperture  $[(20)]$ .

4. (*Currently Amended*) A method as claimed ~~in one of the claims 1 to 3~~, in claim 1, in which the side-walls of the aperture  $[(20)]$  are coated by means of a dielectric material having a low dielectric constant (k).

5. (*Currently Amended*) A method as claimed in claim 4, in which the dielectric material of the coating layer ~~[[22]]~~ is chosen from among fluoruous glass, glass deposited by spinning and silicon oxide containing carbon.

6. (*Currently Amended*) A method as claimed ~~in one of the claims 1 to 5, in claim 1,~~ in which the window of the mask ~~[[18]]~~ registers with at least one active part ~~[[12]]~~ of the substrate, and in which said active part ~~[[12]]~~ of the substrate is exposed during the etching of the intermediate layer of material ~~[[14]]~~ through the window ~~[[18]]~~ of the mask.

7. (*Currently Amended*) A method as claimed ~~in one of the claims 1 to 6, in claim 1,~~ in which apertures ~~[[18]]~~ are etched which extend right through the intermediate layer ~~[[14]]~~.

8. (*Currently Amended*) A method as claimed ~~in one of the claims 1 to 7, in claim 1,~~ in which the mask ~~[[16]]~~ is formed by means of a photolithography technique, and in which the narrowed apertures ~~[[20]]~~ have dimensions (d) which are referred to as "ultimate" dimensions which are smaller than those that can be achieved by means of said photolithography technique.

9. (*Currently Amended*) A method as claimed ~~in one of the claims 1 to 8, in claim 1,~~ in which the ~~connection means~~ electrical connections comprise wiring tracks and/or terminals and/or vias between layers.

10. (*Currently Amended*) An integrated circuit device which comprises ~~connection means~~ electrical connections ~~[[30]]~~ which are embedded in apertures ~~[[20]]~~ of an intermediate layer ~~[[14]]~~ which is flush with an edge of the apertures, said apertures ~~[[20]]~~ having side-walls coated with insulating lateral spacers ~~[[22]]~~, ~~and is realized by means of the method disclosed in one of the claims 1 to 9.~~ the integrated circuit device realized by the method as recited in claim 1.

11. (*Currently Amended*) A device as claimed in claim 10, in which the spacers ~~[[22]]~~ are made of a dielectric material having a low dielectric constant.

12. (*Currently Amended*) A device as claimed ~~in one of the claims 10 or 11~~, in claim 10, in which the ~~connection means~~ electrical connections comprise wiring tracks and/or contact pads and/or vias between layers and have at least one dimension which is smaller than 0.1  $\mu\text{m}$ .

13. (*Currently Amended*) An electrical or electronic device, wireless or not, comprising at least one integrated circuit device as claimed ~~in one of the claims 10 to 12~~. in claim 10.